

ABSTRACT OF THE DISCLOSURE

A semiconductor memory device having a multiport memory includes a plurality of memory cells MC arranged in columns and rows, a plurality of first word lines WLA0-WLAn connected to a first port 13a, and a plurality of second word lines WLB0-WLBn connected to a second port 13b. Each of a plurality of first word lines WLA0-WLAn and each of a plurality of second word lines WLB0-WLBn are arranged alternately in a planar layout. A semiconductor memory device is thus obtained that allows a coupling noise between interconnections to be reduced without an increase in memory cell area.